Section 57 of the Competition Act (Cap. 50B)

Grounds of Decision: Proposed Acquisition by Advanced Micro Devices, Inc. of Xilinx, Inc.

Date: 30 Aug 2021

Case number: 400-140-2021-003

TABLE OF CONTENTS

I. INTRODUCTION

1. On 23 March 2021, Advanced Micro Devices, Inc. ("**AMD**") filed a notification pursuant to section 57 of the Competition Act (Cap. 50B) (the "**Act**") for a decision by the Competition and Consumer Commission of Singapore ("**CCCS**") as to whether the proposed all-stock acquisition by AMD of Xilinx, Inc. ("**Xilinx**") (the "**Proposed Transaction**") will infringe the section 54 prohibition, if carried into effect.

2. In reviewing the Proposed Transaction, CCCS contacted 10 competitors[1] and 20 customers[2] who purchase silicon wafers (collectively referred to as "**third parties**"). Of the third parties contacted, 14[3] responded and 8 provided substantive responses[4]. All of the third parties who responded indicated that they were neutral or have no competition concerns about the Proposed Transaction.

3. At the end of the consultation process and after evaluating all the information, including AMD's and Xilinx's submissions and the feedback provided by third parties, CCCS concludes, on balance, that the Proposed Transaction, if carried into effect, will not infringe section 54 of the Act.

II. THE PARTIES

(a) The Acquirer

AMD

4. AMD is a global semiconductor company headquartered in Santa Clara, California, US, with 40 offices in North America, South America, Asia, Australia, and Europe. AMD is active in the supply of:

   a. Central Processing Units ("**CPUs**") also known as microprocessors, based on the x86 instruction set architecture;

   b. Discrete Graphic Processing Units ("**GPUs**"), which were first introduced to offload simple graphics operations from the CPU, and are currently used for workload acceleration in data centres;

[1] Competitors: [✂]
[2] Customers: [✂]
[3] [✂]
[4] [✂]

c. Accelerated Processing Units ("**APUs**"), which combine a CPU with a discrete GPU; and

d. Semi-custom system-on-chip ("**SoC**") products, that are designed primarily for the gaming console market.

5. AMD offers all products globally, including to customers in Singapore.

(b) The Target

Xilinx

6. Xilinx is a global semiconductor company headquartered in San Jose, California, US, with 12 offices in North America, Europe and Asia Pacific.[5] Xilinx primarily designs and supplies:

a. Field Programmable Gate Arrays ("**FPGAs**") which are a type of programmable logic device that can be configured by customers after fabrication to perform logic and processing tasks;

b. Programmable FPGA-based SoCs and Smart Network Interface Cards ("**SmartNICs**") which combine a FPGA with a processor[6]; and

c. Adaptive Compute Acceleration Platforms ("**ACAPs**") which combine an FPGA, a processor and one or more hardware accelerators[7].

7. Xilinx offers all products globally, including in Singapore.

III. THE PROPOSED TRANSACTION

8. On 27 October 2020, the Parties announced that they had entered into a definitive agreement for AMD to acquire Xilinx in an all-stock transaction valued at US$35

[5] Paragraph 10.10 of Form M1.
[6] An FPGA-based SoC combines a programmable logic core (i.e. the FPGA) with an ARM-based CPU that optimises the FPGA for a specific use. An FPGA-based SmartNIC on the other hand, combines an FPGA with a Network Interface Card. See paragraph 1.11 of Annex 1 of AMD's response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[7] Accelerators can improve processing performance, specifically for compute-intensive applications, such as AI, data analytics, and scientific and engineering computing. See paragraph 2.12 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.

billion (approximately S$46 billion).[8] Pursuant to the agreement and plan of merger by and among AMD, Thrones Merger Sub, Inc., and Xilinx dated 26 October 2020 (the "**Merger Agreement**"), Thrones Merger Sub, Inc., an indirect wholly owned subsidiary of AMD, will merge with and into Xilinx, with Xilinx surviving the merger as a wholly owned indirect subsidiary of AMD.[9] As a result of the Proposed Transaction, AMD will acquire sole control of Xilinx.[10] Based on the Parties' submission, CCCS is of the view that the Proposed Transaction constitutes a merger under section 54(2)(b) of the Act.

IV. COMPETITION ISSUES

9. AMD submitted that there is no horizontal overlap between the Parties' products. CCCS examined the issue and concluded that regardless of whether narrower relevant markets within each processor type are considered, FPGAs (including both standalone FPGAs and FPGA-based products i.e. FPGA-based SoCs, SmartNICs and ACAP) offered by Xilinx, and CPUs, discrete GPUs or semi-custom SoC products offered by AMD are assessed to belong to separate markets.

10. AMD submitted that there are also no vertical relationships between the Parties as each party is not active in markets for any product that is upstream or downstream relative to the products of the other party. Neither AMD nor Xilinx are vertically integrated due to their use of the fabless manufacturing model where they rely on contract manufacturers (i.e., foundries) to manufacture CPUs and FPGAs. No third party has raised any concern in this regard. CCCS agrees with AMD's submission and will not examine this issue further.

11. There is, however, a possible conglomerate relationship between the Parties as (i) CPUs and FPGAs and (ii) discrete GPUs and FPGAs are used, or can be used, together in some servers, in particular in data centres, as well as in some other application segments. CCCS's inquiry found no further conglomerate relationships involving the Parties' products.

12. CCCS assessed whether the conglomerate relationship between the Parties will lead to a substantial lessening of competition ("**SLC**"), including whether the merged entity enjoys significant "portfolio power" and therefore has the ability or incentive to foreclose competitors in any of the affected markets through tying or bundling or to engage in predatory conduct in response to entry or to induce exit

[8] Paragraph 11.1 of Form M1.
[9] Paragraphs 11.2 to 11.3 of Form M1.
[10] Paragraphs 11.2 to 11.3 of Form M1.

by using profits earned in one market to subsidise short-run losses in another market.

V. COUNTERFACTUAL

13. AMD has submitted that, in the absence of the Proposed Transaction, the Parties will continue to operate separately and independently in each of their relevant markets.[11] However, there will be a loss in opportunity for the Parties to rationalise and achieve the efficiencies brought on by the Proposed Transaction.[12]

14. AMD has further submitted that it has not [✂] in the last three years, and has no plans to [✂]. Similarly, Xilinx has not [✂] in the last three years, and has no plans to [✂].[13] [✂].

15. In the absence of third party feedback or evidence suggesting otherwise, CCCS considers the appropriate counterfactual to be the prevailing conditions of competition prior to the Proposed Transaction.

VI. RELEVANT MARKETS

(a) Description of Products

16. CPUs are present in every data centre server and operate as general purpose centralised "brains" of computer systems. They are general purpose processors that are able to perform all types of operations.[14] Typical CPU operations include running software, analysing data, managing networking traffic, fetching data from memory, as well as transferring information to and from other system resources.[15] The majority of CPUs in servers are based on the x86 instruction set architecture, including those used in data centres of all sizes and workloads. CPUs based on other architectures, such as the Advanced RISC Machine ("**ARM**") architecture, have a limited but growing presence in data centres.[16]

[11] Paragraph 25.1 of AMD's Response dated 26 May 2021 to the CCCS's 7 May 2021 RFI.
[12] Paragraph 25.1 of AMD's Response dated 26 May 2021 to the CCCS's 7 May 2021 RFI.
[13] Paragraph 25.2 of AMD's Response dated 26 May 2021 to the CCCS's 7 May 2021 RFI.
[14] Paragraph 2.8 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[15] Paragraph 2.8 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[16] Paragraph 2.9 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.

17. Discrete GPUs were first introduced to offload simple graphics operations from the CPU. Today, discrete GPUs are used for workload acceleration[17] in data centres, including in many of the world's supercomputers. Even though discrete GPUs have more limited capabilities than CPUs, they are much better suited to processing graphic images or computations that require massive parallel execution of relatively simple computational tasks.[18]

18. FPGAs are a type of programmable logic device ("**PLDs**") that offer customers a wide range of logic capacity, features, speed, and voltage characteristics. PLDs include complex programmable logic devices ("**CPLDs**") and FPGAs. CPLDs are integrated circuits that can be configured by customers and are primarily used as "glue logic" to interface with other integrated circuits in a system.[19] FPGAs can also be configured by customers after fabrication to perform logic and processing tasks. The ability to reprogramme FPGAs with desired application or functionality requirements after manufacturing (i.e., "in the field") distinguishes them from other accelerators.[20] The ability to reconfigure and optimise a FPGA for a particular set of functions makes it an attractive option for applications with evolving standards and algorithms.[21]

19. AMD also submitted that FPGA-related products, namely, FPGA-based SmartNICs, FPGA-based SoCs, and FPGA-based ACAPs all contain FPGAs that can be programmed, and therefore in many cases can be used as substitutes for standalone FPGAs in data centres.[22] Network interface cards ("**NICs**" or network adapters) are typically used in a server, enabling it to communicate with other devices on a network.[23] SmartNICs integrating FPGA technology allow data centre operators to reconfigure the NIC to support new functions or protocols.[24] FPGA-based SoCs are similar to SmartNICs in that they combine a programmable logic core (i.e., the FPGA component) with another component (i.e., a NIC for SmartNICs and an ARM-based CPU for SoCs) that optimises the FPGA for a

[17] Data centres consist of a collection of servers that are connected by a network and that work together to process or "compute" workloads. A workload refers to a computer system's ability to handle and process workloads and data. For example, every time someone makes a search online, a workload is processed by a data centre that finds and presents the search results. Devices that are used in data centres to process data include CPUs and in some cases accelerators. The type of device used to process data varies depending on factors such as the data centre's intended applications (i.e., workload acceleration), performance demands, price and other customer needs and preferences. See paragraph 2.2 and 2.7 of AMD's 16 April 2021 Response to CCCS's 30 March 2021 RFI.
[18] Paragraph 2.16 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[19] Paragraph 2.17 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[20] Paragraph 2.18 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[21] Paragraph 2.18 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[22] Paragraph 1.2 of Annex 1 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[23] Paragraph 2.22 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[24] Paragraph 2.24 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.

specific use.[25] Lastly, FPGA-based ACAPs are fully software-programmable, multi-core heterogeneous compute platforms which combine a FPGA component, a processor and one or more additional hardware accelerators.[26] ACAPs are adaptable and can accelerate functions at which the CPUs are inefficient e.g., storage processing, video transcoding, and network offloading. [27]

(b) Product Markets

AMD's submissions

CPUs

20. AMD submitted that in *Intel/Altera*[28], the European Commission ("**EC**") defined a separate product market for all CPUs but left open the question as to whether the market should be further segmented according to (i) the architecture used (x86 CPU vs. non-x86 CPU); and (ii) the types of device (desktop, laptop, or server). The EC's market investigation had indicated that a possible segmentation of CPUs based on the types of device into which they are incorporated (e.g., servers, desktops, or laptops) may be appropriate due to differentiated price, functionality, performance, power, architecture extensions and flexibility. Mixed views were expressed to the EC by third parties as to whether segmentation according to the architecture used (e.g., x86 architecture vs. ARM, Power, MIPS, SPARC, GP-GPU, or other architecture) would be appropriate for all types of end devices. Ultimately, the EC declined to further segment the market for all CPUs, since the transaction did not raise competition concerns even on the narrowest market definition.[29]

21. AMD submitted that the Parties do not dispute the EC's approach taken in *Intel/Altera* insofar as the EC determined that a single relevant product exists encompassing all CPUs, but that further segmentation might be appropriate. However, the Parties are of the view that the question of whether the relevant product market for CPUs should be segmented according to (i) the architecture used or (ii) the types of device into which the CPU is incorporated, can be left open, since the Proposed Transaction does not raise any competition concerns no matter the exact market definition used.[30] Further, even if CPUs for servers

[25] Paragraph 1.11 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[26] Paragraph 4.3 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[27] Paragraph 4.4 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[28] Case No M.7688 – Intel/Altera Commission decision pursuant to Article 6(1)(b) of Council Regulation No 139/2004 and Article 57 of the Agreement on the European Economic Area
[29] Paragraph 5.5 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[30] Paragraph 5.6 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

constitute a separate relevant product market, there is no basis for a further segmentation of the market based on the application for which the server or CPU is used (e.g., data centres or high-performance computing).[31]

22. AMD also submitted that the competitive assessment remains the same whether the wider server CPUs or the narrower x86 server CPUs is the relevant market, because x86 server CPUs make up all but a tiny percentage of the wider market for server CPUs (i.e., x86 server CPUs make up the majority of the wider market for server CPUs).[32]

APUs

23. AMD submitted that APUs should be included in the same relevant product market as CPUs as APUs are examples of SoCs (comprising of a CPU and a built-in discrete GPU) in which the principal element in APUs is the CPUs. [33] In any case, AMD submitted that AMD's APUs are not used in the server market and accordingly not used as substitutes to CPUs in data centres. Furthermore, the Parties are not aware of any instances where APUs and FPGAs are used together outside of data centres.[34]

FPGAs

24. AMD submitted that in *Intel/Altera*, the EC considered whether a further segmentation should be made between different types of FPGAs[35]. The EC considered the following possible segmentations within the market for FPGAs: (i) segmentation based on performance characteristics (i.e., between high-end, mid-range, and low-cost devices); (ii) segmentation based on the type of device into which FPGAs are installed (i.e., desktops, laptops, and servers); and (iii) within the FPGAs server segment, a further segmentation based on the FPGA's intended use. On the last point, the EC considered whether FPGAs for servers could be distinguished based on whether they were intended to be used for (a) computing, (b) networking, or (c) storage; and (d) within computing, whether workload acceleration was a separate relevant product market.[36]

25. Ultimately, the EC left open the question as to whether the market for FPGAs should be further segmented according to: (i) performance characteristics; (ii) type

[31] Paragraph 5.7 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[32] Paragraph 5.8 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[33] Paragraph 1.2 of Annex 2 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[34] Paragraph 1.1 of Annex 2 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[35] EC's Intel/Altera decision did not make any distinction or references to standalone FPGAs or other FPGA-related products such as FPGA-based SoCs, ACAPs and FPGA-based SmartNICs.
[36] Paragraph 5.9 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

of device into which the FPGA is incorporated; and (iii) the intended use of the FPGA, given that the transaction did not raise serious competition concerns even on the narrowest possible product market.[37]

26. AMD submitted that the Parties agree with the EC that the exact scope of product market definition for FPGAs[38] can be left open as the Proposed Transaction does not raise competition concerns under any plausible definition. The Parties also do not believe that the market for FPGAs should be further segmented based on performance characteristics, type of device, or intended use (in particular, as between computing, networking, or storage in a data centre), given that – as noted in *Intel/Altera* – FPGAs are generic, programmable logic devices that can serve all three purposes. FPGAs used in data centres are off-the-shelf products that can be used in a variety of applications (i.e., there are no "data centre only" FPGAs).[39]

No horizontal overlap between Parties' products

27. AMD submitted that there is no horizontal overlap between the products supplied by the Parties.[40] AMD's submissions on the distinctions between the Parties' key products are set out in the paragraphs below.

28. *CPUs and FPGAs.* AMD submitted that Xilinx's FPGAs (including standalone FPGAs, FPGA-based SoCs, ACAPs and FPGA-based SmartNICs)[41] cannot effectively be used as substitutes for AMD's CPUs in any applications.[42] CPUs are optimised for general purpose computing and sequential processing. Although FPGAs can, as a purely technical matter, be programmed to do similar computational tasks, they are not realistically or functionally a substitute for CPUs because of differences in terms of energy consumption, cost and/or performance. AMD submitted that this is supported by the market feedback received by the EC during its review of the Proposed Transaction which stated that FPGAs are almost never credible alternatives to CPUs and that any substitution between these chips is limited to specific applications.[43]

[37] Paragraph 5.10 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[38] All reference to "FPGAs" in AMD's submission regarding the relevant product markets relates to all FPGAs, including standalone FPGAs, FPGA-based SmartNICs, FPGA-based SoCs and ACAPs. See paragraph 2.3 of AMD's Response dated 28 June 2021 to CCCS's 15 June 2021 RFI.
[39] Paragraph 5.11 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[40] Paragraph 5.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[41] Paragraph 2.3 of Annex 2 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[42] Paragraph 2.1 of Annex 2 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[43] Paragraph 2.1 of Annex 2 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.

29. *Discrete GPUs and FPGAs.* AMD submitted that there is no horizontal overlap in respect of discrete GPUs and FPGAs, and they cannot be considered substitutes in any applications in any industry, including as accelerators in data centres. Although AMD's discrete GPUs and Xilinx's FPGAs can both be used in data centres for workload acceleration, the Parties' product offerings are highly differentiated (and not complementary) in terms of functionality, application scenarios, application fields, customisability, prices, computing efficiency, performance metrics, and power consumption.[44]

30. AMD further submitted that FPGAs and such other acceleration technologies[45] (i.e., discrete GPUs, ASICS, ASSPs[46]) have distinct characteristics, which means they are each well suited to their specific types of acceleration task in data centres while being poorly suited to others.[47] In the case of discrete GPUs and FPGAs, the key difference is that discrete GPUs are suited to parallel processing of data from memory and executing relatively simple computational tasks (such as processing images), while FPGAs are suited to sequential processing of data flow tasks streaming in from a device involving unstructured data and complex computations.[48] In this regard, AMD also submitted that the EC has acknowledged in *Nvidia/Mellanox*[49] that different accelerators are generally suitable for different applications in data centres[50]:

"[…] competitors, OEMs and most end customers consider different types of accelerators to be suitable for different kinds of HPC[51] *and deep learning applications. They are therefore likely not part of the same market […]."*[52]

CCCS's assessment

[44] Paragraph 1.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[45] Accelerators can improve processing performance, specifically for compute-intensive applications, such as AI, data analytics, and scientific and engineering computing. See paragraph 2.12 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[46] Other than discrete GPUs and FPGAs, application specific integrated circuits ("ASICs") and application specific standard products ("ASSPs") are also used as accelerators. ASICs are custom designed for a single purpose which remains the same for the duration of their operating life. Unlike FPGAs, which are reprogrammable, the logic function of an ASIC cannot be changed to anything else. In this regard, ASICs are best suited for high-volume applications. ASSPs are designed and implemented in the same way as ASICs but are a more of a general-purpose device. Whereas ASICs are customised for use by a specific customer, ASSPs are "off-the-shelf" products that can be purchased in identical form by a number of different customers. See paragraph 2.19 and 2.20 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[47] Paragraph 2.56 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[48] Paragraph 1.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[49] Case M.924 – Nvidia/Mellanox Commission decision pursuant to Article 6(1)(b) of Council Regulation No 139/2004 and Article 57 of the Agreement on the European Economic Area
[50] Paragraph 2.13 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[51] High performance computing.
[52] Paragraph 27 of EC's Nvidia/Mellanox (Case M.9424).

31. CCCS is of the view that the exact scope of the product market definition for CPUs, FPGAs and discrete GPUs can be left open as the competition assessment in the subsequent section shows that the Proposed Transaction does not raise competition concerns under any of the considered market definitions. CCCS also agrees that APUs could be included in the same relevant product market as CPUs given that the principal element in an APU is the CPU. CCCS did not receive any third party feedback to suggest otherwise.

32. CCCS also notes that third party feedback generally agrees with AMD's submission that AMD's products (i.e., CPUs and discrete GPUs) and Xilinx's FPGAs (i.e., standalone FPGA[53], FPGA-based SoCs[54], FPGA-based SmartNICs[55] and ACAPs[56]) are distinct and not substitutable.

(c) Geographic Market

AMD's submissions

33. AMD submitted that the relevant geographic market for CPUs and FPGAs is worldwide.[57] This is in line with CCCS's and the EC's prior decisions in the semiconductor industry where the relevant geographic markets are defined to be worldwide in scope given the global nature of supply and demand irrespective of the location of the component vendor or the location of the end customers.[58] AMD also submitted that those decisions were based on similar factors to those of the Proposed Transaction[59]:

[53] [✂] to Question 6 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 6 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 6 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 6 of CCCS's Invitation to Comment dated 31 May 2021. [✂] to Question 4 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 5 of CCCS's Invitation to Comment dated 17 May 2021.
[54] [✂] to Question 4biii and 6 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 7 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 7 of CCCS's Invitation to Comment dated 31 May 2021. [✂] to Question 4b of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 6 of CCCS's RFI dated 17 May 2021.
[55] [✂] to Question 6 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 7 of CCCS's Invitation to Comment dated 31 May 2021. [✂] to Question 4b of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 5 of CCCS's Invitation to Comment dated 17 May 2021.
[56] [✂] to Question 6 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 4biv and 7 of CCCS's Invitation to Comment dated 31 May 2021. [✂] to Question 4b of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 5 of CCCS's Invitation to Comment dated 17 May 2021.
[57] Paragraph 6.5 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[58] Paragraph 6.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[59] Paragraph 6.3 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

"*[…] customers are generally able to source from different suppliers without any geographical constraints. The portion of transportation cost to the product price is immaterial and the difference in prices of the same product between different territories is negligible, as transportation and distribution costs across geographical borders are low and trade barriers are marginal*."[60]

"*[…] suppliers and customers […] supply and source their products and services around the world and consequently have branches worldwide […] the supply of the Parties' products may not be constrained by the location of the suppliers' business operations*."[61]

CCCS's assessment

34. Third party feedback generally corroborates AMD's submissions that customers source CPUs and FPGAs and any other complementary products on a worldwide basis.[62] From the customers' perspective, sourcing decisions are based on product and supplier requirements, rather than the location of the suppliers.[63] Similarly, suppliers indicated that they supply CPUs and FPGAs on a global basis.[64] [65] CCCS is therefore of the view that the relevant geographic market for CPUs, discrete GPUs and FPGAs is likely to be worldwide to worldwide but considers that it is not necessary to conclude on the precise definition of the geographic market as it does not affect the competition assessment of the Proposed Transaction.

(d) Overall Assessment on Relevant Markets

35. CCCS is of the view that it is not necessary to conclude on the precise definition of the relevant markets as it does not affect the competition assessment of the Proposed Transaction. CCCS will therefore assess the competition impact of the Proposed Transaction based on the following possible relevant markets:

[60] CCCS 400/003/17 Proposed Acquisition by SK Holdings Co. Ltd. Of LG Siltron, paragraph 64.
[61] CCCS 400/005/16 Proposed Acquisition by ASML Holding N.V. of Hermes Microvision, Inc., paragraph 50 and 51.
[62] [✂] to Question 11 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 11 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 11 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 11 of CCCS's Invitation to Comment dated 31 May 2021. [✂] to Question 9 and 26 of CCCS's Invitation to Comment dated 17 May 2021.
[63] [✂] to Question 12 of CCCS's Invitation to Comment dated 31 May 2021.
[64] [✂] to Question 10 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 9 of CCCS's Invitation to Comment dated 17 May 2021.
[65] [✂] to Question 10 and 11 of CCCS's Invitation to Comment dated 17 May 2021.

a. Worldwide-to-worldwide supply of FPGAs with possible further segmentation by types of FPGAs (i.e., standalone FPGAs, FPGA-based SoCs, FPGA-based SmartNICs, ACAPs), performance characteristics and application segments (i.e., data centres and other segments);

b. Worldwide-to-worldwide supply of CPUs (including APUs) with possible further segmentation by architecture and application segments; and

c. Worldwide-to-worldwide supply of discrete GPUs with possible further segmentation by application segments.

VII. MARKET STRUCTURE

36. Based on AMD's submissions, AMD has a market share of [0-10]% in the x86 CPUs data centre segment, and less than [0-10]% market share in all other considered application segments in the market for CPUs outside data centres in 2020. In all the considered application segments, including data centres, AMD has insignificant market shares in the markets for discrete GPUs (e.g. [0-10]%) in 2020. Xilinx has about [40-70]% market share in the market for FPGAs (depending on the market segment by performance characteristics), [50-60]% market share in the data centre segment and [30-70]% in the other considered application segments in 2020.

VIII. COMPETITION ASSESSMENT

Possible complementary relationship between FPGAs and (i) CPUs/APUs and (ii) discrete GPUs

AMD's submissions

37. AMD submitted that AMD's CPUs and Xilinx's FPGAs perform complementary functions in data centres and can be purchased by the same set of customers.[66] While AMD does not consider CPUs and FPGAs as complements outside of the data centre segment based on its understanding on how these industries operate,[67] AMD notes that theoretically, there may also be areas outside of the data centre segment – which include (i) security space (security appliance or security enabled routers), (ii) wireless and wired space (wireless infrastructure in virtualized radio access networks, and wired core networks and routers for control plane

[66] Paragraph 2.1 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[67] Paragraph 1.5 of AMD's Response dated 10 June 2021 to CCCS's 3 June 2021 RFI.

processing), (iii) aerospace and defence space, (iv) automotive space, (v) medical imaging, and (vi) industrial controls [68] – where a Xilinx FPGA could be used as a hardware accelerator with an AMD processor.[69] AMD and Xilinx have the technical capability to reconfigure their chips such that AMD's CPUs and Xilinx's FPGAs could perform complementary roles in these segments.[70] Thus far, AMD is only aware of a single example of a customer purchasing an AMD CPU and a Xilinx FPGA for application outside of the data centre segment.[71] While AMD is aware of Intel attempting to market its FPGA product as a bundled solution with a CPU in the wireless space[72], AMD notes that customers usually purchase CPUs and FPGAs independently through distributors and it is not aware if any customer actually buys or uses such a bundled solution in practice.[73]

38. Other than CPUs and FPGAs (including both standalone FPGAs and FPGA-related products), AMD does not consider that any other products supplied by AMD and Xilinx respectively, can be considered as complements in data centres or in other applications or industries.[74] AMD submitted that no conglomerate relationship arises between discrete GPUs and FPGAs[75].

CCCS's assessment

39. Third party feedback confirmed that AMD's CPUs and Xilinx's FPGAs (including both standalone FPGAs and FPGA-related products) are used complementarily in data centres as well as certain other applications outside data centres (e.g. security space, wireless and wired space, aerospace and defence space, automotive space, medical imaging, and industrial controls).

40. All customers who responded to CCCS's enquiries confirmed AMD's submission that FPGAs and discrete GPUs are not complementary. Almost all competitors also did not consider FPGAs and discrete GPUs to be complementary.

41. Based on the Parties' submission and third party feedback, CCCS considers that (i) CPUs (including APUs used in place of CPUs where relevant) and FPGAs are used, or can be used together in some servers, in particular in data centres, as well as in a number of application segments outside data centres; while (ii) use of

[68] Paragraph 3.3 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[69] Paragraph 5.4 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[70] Paragraph 3.4 of AMD's Response dated 28 June 2021 to CCCS's 15 June 2021 RFI.
[71] Paragraph 5.4 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[72] Paragraph 3.4 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[73] Paragraph 1.5 of AMD's Response dated 10 June 2021 to CCCS's 3 June 2021 RFI.
[74] Paragraph 3.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[75] Paragraph 5.1.3 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

discrete GPUs and FPGAs are not likely complementary whether in or outside data centres, although CCCS considers that it is not necessary to come to a definitive view given that competition concerns are not likely to arise even if such a complementary relationship exists.

(a) Ability and incentive to foreclose FPGAs competitors through "portfolio power"

AMD's submissions

42. AMD submitted that the merged entity will have neither the ability nor the incentive to leverage its minor market position in the market for server CPUs to the closely related market for FPGAs for data centres. AMD's share of the market for server CPUs was [0-10] % in 2020 compared to Intel which holds [90-100] % market share. With AMD's small market share, it does not have any market power in the market for server CPUs that AMD can leverage on in the market for FPGAs. Any attempt to create a tying arrangement between CPUs and Xilinx's FPGAs post-Proposed Transaction would not be capable of foreclosing Intel or any other FPGAs supplier from the data centre application segment, given AMD's very small presence on the hypothetical tying market. Moreover, even if the merged entity tied Xilinx's FPGAs and AMD's server CPUs post-Proposed Transaction, third party non-x86 server CPUs, such as ARM-based processors, could be paired with Intel's FPGAs by data centre customers, given that Intel has continued supplying FPGAs to its rivals in the CPUs market since acquiring Altera in 2015.[76]

CCCS's assessment

43. CCCS notes that AMD does not have significant worldwide to worldwide market share in any of the markets for CPUs or discrete GPUs. As such, it will not be able to leverage its position in these markets to foreclose Xilinx's competitors in the markets for FPGAs post-Proposed Transaction.

44. CCCS notes AMD's submission that regardless of the market definition adopted, Intel is the largest global supplier with worldwide to worldwide market shares of [90-100]% for the supply of all CPUs and x86 CPUs used in data centres in 2020 respectively.[77] Although AMD is the second largest global supplier, its worldwide to worldwide market shares for the supply of all CPUs and x86 CPUs used in data centres in 2020 are significantly smaller than that of Intel's. In relation to each of

[76] Paragraph 27.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[77] Paragraph 27.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

the other considered application segments, CCCS notes that AMD's market shares for CPUs remained negligible (i.e., less than [0-10]%) across the last 3 years. Even if APUs are considered separately, CCCS notes that AMD's worldwide to worldwide market shares for APUs in all considered applications outside of data centres are similarly insignificant across the past 3 years.[78] Accordingly, the merged entity is unlikely to be able to leverage AMD's market position in the relevant markets for CPUs to foreclose competition in any other market (e.g. the market for FPGAs). Likewise, CCCS notes that AMD has an insignificant worldwide to worldwide market shares for discrete GPUs in data centres as compared to Nvidia.

45. Third party feedback indicated that CPUs and FPGAs are not commonly purchased as a portfolio or bundle. Customers indicated a strong preference for a "mix and match" approach and would be reluctant to buy as a bundle at the expense of performance and efficiency considerations. Given such preference by customers, the merged entity is unlikely to have the incentive to tie or bundle CPUs and FPGAs given the risk of loss of standalone sales. Please see further discussion below at paragraphs 73 to 75.

(b) Ability and incentive to foreclose competitors in the markets for CPUs and discrete GPUs through "portfolio power"

AMD's submissions

46. AMD submitted that the merged entity will have no ability to leverage its position in the market for FPGAs to foreclose competitors in the market for CPUs, both in the data centre space and in any other application segment through contractual tying/bundling, technical tying and mixed bundling.

47. AMD submitted that the merged entity will still face a competitor of comparable size in the FPGAs segment (Intel) which is also an overwhelmingly dominant rival in the server CPUs segment and which enjoys the advantage of being vertically integrated unlike the merged entity. As CPUs are the essential core of every server and the choice of CPUs is the primary architectural decision when designing a data centre, Intel's undisputed market power in relation to server CPUs matters far more than any supposed market power that Xilinx may have in relation to FPGAs.[79] The market for CPUs used in data centres is more than [✂] times the

[78] AMD submitted that APUs are not deployed in data centres and its market share is accordingly 0%. In the industrial controls segment which AMD has the highest sales of APUs, CCCS notes that AMD's market shares in this segment was only [0-10] % in 2020.
[79] Paragraph 2.30 of AMD's Response dated 16 April 2021 Response to CCCS's 30 March 2021 RFI.

size of the data centre market for FPGAs[80]. Intel manufactures a majority of its products in its own facilities and make significant investments in silicon manufacturing technologies and platforms as an integrated device manufacturer, in contrast to AMD and Xilinx's fabless manufacturing model[81], and has more control over prioritisation and production of its CPUs and FPGAs than the Parties, allowing Intel to unilaterally decide to allocate more or less resources to a particular product in reaction to various extrinsic stresses.[82]

48. AMD submitted that since demand for CPUs is much larger than the demand for FPGAs, there are plenty of opportunities for CPU-only suppliers to sell CPUs to customers who do not buy FPGAs, and/or for applications that do not require a FPGA. In this regard, AMD submitted that [✂] of its data centre customers do not deploy standalone FPGAs or FPGA-based SoCs in volume in data centres.[83] Thus any tying or bundling by the merged entity would not impact competition among CPUs suppliers or make it more difficult for rival CPUs suppliers to compete. This is especially the case because Intel dominates the market for CPUs generally and the market for CPUs used in data centres specifically. Therefore, the merged entity would not be able to influence a significant part of the demand for CPUs by leveraging Xilinx's position in the market for FPGAs, nor generate other conglomerate effects.[84]

49. To the best of AMD's knowledge, neither AMD nor Xilinx have engaged in, or are engaged in, any collaboration or joint bidding involving the bundling of their respective products to common customers.[85]

50. AMD also submitted that the use of open standards, such as the Peripheral Component Interconnect Express ("**PCIe**") interconnect technology[86], helps facilitate new entry by ensuring interoperability between the new entrant's device (e.g. FPGA) and other components in a server supplied by third parties.[87] AMD submitted that the industry is moving towards greater interoperability. This

[80] Paragraph 27.7 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[81] Paragraph 1.2 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[82] Paragraph 11.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[83] Paragraph 12.1 of AMD's Response dated 28 June 2021 to CCCS's RFI dated 15 June 2021 and paragraph 3.1 of Annex 2 of AMD's Response dated 28 July to CCCS's RFI dated 2 July 2021.
[84] Paragraph 1.6 of Annex 1 of AMD's response dated 28 July 2021 to CCCS's RFI dated 2 July 2021.
[85] Paragraph 3.4 of AMD's response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[86] PCIe slots are used to connect the CPU to other peripherals within a server. PCIe is an open standard available to everyone on FRAND terms, and it is the de facto standard for interconnecting systems within a server. The PCIe standard ensures interoperability between CPU and other components in servers. See paragraph 2.10 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 RFI.
[87] Paragraph 18.10 of the Form M1.

reflects significant pressure from customers, particularly hyperscalers[88], that want open standards to ensure the greatest level of interoperability throughout the technology stack so that the data centres they build can incorporate technology and components from the full range of suppliers.[89] AMD submitted that the industry-wide push for interoperability means that vendors of semiconductor devices (including Intel and the merged entity) have a strong commercial incentive to ensure that their components can connect and work with components from third party suppliers.[90]

51. AMD submitted that no conglomerate effect arises from AMD's supply of discrete GPUs and Xilinx's supply of FPGAs. While AMD's discrete GPUs and Xilinx's FPGAs can both be used in data centres for workload acceleration, the Parties' product offering are highly differentiated (and therefore not complementary) in terms of functionality, application scenarios, application fields, customisability, prices, computing efficiency, performance metrics, and power consumption.

CCCS's assessment

52. CCCS considers that the merged entity will not have the ability and incentive to foreclose rival suppliers of CPUs by means of contractual tying or bundling, mixed bundling or technical tying.

53. First, under any of the considered market definitions for FPGAs and CPUs, the common pool of customers (i.e. sourcing both FPGAs and CPUs) is relatively small compared to the overall number of CPUs customers. The total market size for server CPUs was about [✂] times larger than the total market size for FPGAs in data centres in 2020. Therefore the merged entity would not be able to influence a significant part of the demand for CPUs by leveraging on Xilinx's position in the market for FPGAs.

54. Supporting this point, many third party respondents submitted that FPGAs and CPUs are only used complementarily in limited applications and by a small number of users, and the number of CPUs used together with FPGAs account for a small proportion of all CPUs.

[88] According to AMD, hyperscalers include Alibaba, Amazon, Apple, Google, and Microsoft. See paragraph 2.50 of AMD's Response dated 16 April 2021 to CCCS's RFI dated 30 March 2021.
[89] Paragraph 8.3 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[90] Paragraph 8.4 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

55. Accordingly, CCCS is of the view that given the low rate of common usage and the small pool of common customers, any bundling or tying strategy by the merged entity would still leave a large portion of the market for CPUs unaffected (under any of the considered market definitions). Hence significant opportunities remain for CPUs suppliers to sell CPUs on a standalone basis and their sales are unlikely to be adversely impacted even if the merged entity bundled or tied the sales of its CPUs and FPGAs.

56. Second, although Xilinx may have significant market shares in the market for FPGAs, including certain possible market segments being considered, CCCS is of the view that the presence of a strong competitor (i.e., Intel) and other smaller FPGAs suppliers (such as Lattice, MicroChip and Achronix) will impose effective competitive constraints on Xilinx, which have not been identified by third parties as an unavoidable trading partner in any of the FPGA-related markets.

57. In this regard, third party respondents have confirmed that the presence of alternative suppliers for customers to switch to would constrain the merged entity with regard to any attempt to bundle its CPUs and FPGAs. Customers submitted that they are currently able to switch between competing manufacturers of CPUs and FPGAs and do not believe the Proposed Transaction will make it more difficult to switch their purchase of CPUs or FPGAs either from manufacturers that supply both or from manufacturers that supply only one of the products.[91]

58. CCCS also examined if rivals faced capacity constraints which in turn would weaken their competitive constraint on the merged entity. All suppliers of FPGAs except Intel (Xilinx's main FPGAs competitor) follow the fabless model (i.e., they outsource manufacturing as they do not own any manufacturing assets). There is currently a global semiconductor shortage due to capacity constraints at the manufacturing level. This global shortage, while affecting competing FPGAs suppliers, similarly affects Xilinx. On the other hand, Intel, Xilinx's main FPGAs rival, is likely to be in a stronger position as it has its own manufacturing facilities and has recently announced its plans to invest a total of over USD$20 billion to expand its capacity for CPUs and FPGAs.[92]

59. Further, Intel, the merged entity's main CPU and FPGA competitor, could similarly replicate comparable CPU-FPGA bundles. Intel clearly enjoys a stronger market position than AMD as evident from its worldwide to worldwide market

[91] [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021.
[92] [✂] to Question 22 of CCCS's Invitation to Comment dated 17 May 2021.

shares for CPUs. In addition, AMD has a weak market position (e.g., less than [0-10] % market shares in 2020) in the other market segments under the considered market definitions for CPUs. This suggests that the foreclosure effects of bundling/tying strategies on Intel is likely to be minimal.

60. Third, third party feedback indicated that the bundling of CPUs and FPGAs is not a market practice and does not appear likely. Customers indicated a strong preference for a "mix and match" approach and would be reluctant to buy as a bundle at the expense of performance and efficiency considerations. Customers will only adopt a bundled solution if it delivers both cost savings and optimal performance and efficiency levels for a given application.

61. Customers have likewise expressed no concerns over possible technical bundling by the merged entity. Given customers' strong preference for open interconnect standards which will enable them to "mix and match", any attempt to degrade compatibility with PCIe by the merged entity is likely to lead to customers choosing devices offered by other suppliers and does not appear to be an effective foreclosure strategy. CCCS's assessment on the countervailing buyer power (see paragraphs 73 to 75) below also confirms that customers are generally able to switch between different suppliers of CPUs and FPGAs and they multi-source from a number of suppliers.

62. The fact that Intel did not pursue a bundling/tying strategy following its merger with Altera (a FPGAs producer) in 2015 (even in the face of losing some market share to AMD in the last two years) further supports the point that this is not a feasible commercial strategy.

63. Fourth, given the limited portion of the market for CPUs attributable to customers who also use FPGAs and customers' strong preference for "mix and match" and open interconnect standards to achieve optimal performance and efficiency levels, it is questionable whether a tying or bundling strategy would be profitable for the merged entity particularly since Xilinx's FPGAs have not been identified as a "must-have" by customers.

64. For completeness, CCCS considered that any complementary relationship between FPGAs and discrete GPUs (and therefore conglomerate effects) is unlikely to adversely impact competition as the merged entity is unlikely to have the ability or incentive to foreclose competitors in discrete GPUs by leveraging on any potential market power in FPGAs given that:

a. The small extent of common usage of FPGAs and discrete GPUs (see discussion at paragraph 40 above) means any attempted tying and bundling is even less likely (than in the case of FPGAs and CPUs) to impact the market for discrete GPUs meaningfully.

b. The merged entity will continue to be constrained by other FPGAs competitors (such as Intel) in the market for FPGAs (see paragraphs 56 to 59 above) and will also face a strong competitor (i.e., Nvidia) in the discrete GPUs market.

c. As with the case of CPUs and FPGAs, customers' preference for a mix-and-match approach and open interconnect standards would reduce the incentive to bundle or tie given the risk of loss of standalone sales.

65. In summary, CCCS considers that the Proposed Transaction will not lead to a substantial lessening of competition resulting from the conglomerate effects arising from the merged entity supplying CPUs, discrete GPUs and FPGAs.

66. CCCS adds that the above assessment also indicates that it is unlikely for the merged entity to be able to engage in predatory conduct which requires the merged entity to leverage its market power in one or more of the relevant markets, especially in the presence of a strong competitor in Intel with a much stronger position in the larger market for CPUs.

67. For completeness, notwithstanding the finding that the Proposed Transaction will not lead to a substantial lessening of competition resulting from the conglomerate effects arising from the merged entity, CCCS has proceeded to further consider the ability of customers to exercise countervailing buyer power and the possibility of entry constraining the conglomerate supplier (i.e. the merged entity).

(c) Countervailing Buyer Power

AMD's submissions

68. AMD submitted that the Parties will continue to face significant buyer power from large and sophisticated customers and consequently would not have the ability nor incentive to foreclose competition either globally or in Singapore.[93]

[93] Paragraph 2.51 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.

69. AMD submitted that its customer base is [✂].[94] In the overall CPUs segment, AMD's top ten customers represent approximately [✂]% of its total CPUs revenue, while AMD's top ten server CPUs customers represent approximately [✂]% of its total server CPUs revenue. They therefore have significant commercial leverage vis-à-vis AMD.[95] AMD's top 10 server CPUs end customers include large companies which have strong market expertise, dedicated procurement teams and significant buyer power.[96]

70. AMD submitted that Xilinx's customer base is [✂].[97] In the FPGAs segment, its top ten customers globally represent approximately [✂]% of its total FPGAs revenue and have significant leverage vis-à-vis Xilinx in the FPGAs space.[98] Particularly in the data centre space, Xilinx's top global customers are hyperscalers that represent approximately [✂]% of Xilinx's revenues in the data centre space, as well as large multinational enterprises that represent another approximately [✂]% of Xilinx's data centre revenues.[99] These hyperscalers and enterprise customers all have strong market expertise and dedicated procurement teams.[100]

71. AMD submitted that customers tend to replace overall systems when systems reach the end of their lifecycles and generally do not replace individual components such as the CPUs or FPGAs used during the middle of a system's lifecycle because it is more efficient and less costly to replace multiple components at once when putting together a new system than to change individual components during a system's lifecycle.[101] AMD submitted that the average lifecycle of CPUs and FPGAs used in data centres is two to four years, and three to four years respectively.[102] Customers however have the opportunity to consider switching semiconductor device suppliers between lifecycles. Notwithstanding this, AMD submitted that it is feasible for customers to switch suppliers for a single component within the device's lifecycle if the customer so desires.[103]

72. AMD generally does not impose contractual impediments that would prevent a customer from switching server CPUs suppliers during the contractual period.[104]

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[94] Paragraph 2.49 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[95] Paragraph 2.49 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[96] Paragraph 2.49 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[97] Paragraph 2.50 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[98] Paragraph 2.50 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[99] Paragraph 2.50 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[100] Paragraph 2.50 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[101] Paragraph 18.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[102] Paragraph 9.1 of AMD's Response dated 28 June 2021 to CCCS's 15 June 2021 RFI.
[103] Paragraph 18.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI
[104] Paragraph 16.5 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

Xilinx is similarly not aware of any contractual impediments to switching for FPGAs.[105] To the best of AMD's knowledge, all of AMD's server CPUs customers also buy Intel's server CPUs.[106] AMD further submitted that it has never been the exclusive supplier of server CPUs for any of its customers in the past five years.[107] AMD submitted that at this time, self-supply is unlikely to be an economical choice for most smaller customers given the cost of developing and designing semiconductor products such as CPUs and FPGAs.[108]

CCCS's assessment

Customer switching

73. Third party feedback generally indicates that switching between different suppliers of CPUs and FPGAs is possible, especially if the decision to switch is taken at the point of the design of the architecture of the server product systems.[109] Feedback also indicates that it is also easy to switch between CPUs and FPGAs to the extent that the server and other components can be designed/customised to work with the various CPUs and FPGAs offered by different manufacturers.[110] If the decision to switch is taken after this point, significant switching costs in the form of software replacement costs for instance, may be incurred.[111] It is also not easy to switch CPUs and FPGAs products within a specific server design.[112]

74. In terms of the duration of the lifecycle of CPUs and FPGAs, third party feedback is mixed.[113] Feedback from one third party suggests that the frequency with which CPUs and FPGAs would need to be replaced (which affects the lifecycle of the CPUs and FPGAs) is dependent on the workload required of the CPUs and FPGAs.[114] Feedback provided by third parties generally indicated that they have

[105] Paragraph 16.6 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[106] Paragraph 17.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[107] Paragraph 17.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[108] Paragraph 20.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[109] All third parties who responded indicated that switching between different suppliers of CPUs and FPGAs is possible, with the exception of two. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 16 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 28 to CCCS's Invitation to Comment dated 17 May 2021.
[110] [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021.
[111] [✂] to Question 16 of CCCS's Invitation to Comment dated 17 May 2021.
[112] [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021.
[113] [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 21 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 21 of CCCS's Invitation to Comment dated 17 May 2021. [✂] of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 21 of CCCS's Invitation to Comment dated 17 May. [✂] to Question 32 of of CCCS's Invitation to Comment dated 17 May. [✂] to Question 21 of CCCS's Invitation to Comment dated 17 May 2021.
[114] [✂] to Question 22(b) of CCCS's Invitation to Comment dated 17 May 2021.

not experienced any difficulties (e.g. technical/interoperability difficulties) in pairing CPUs and FPGAs offered by different manufacturers (e.g. between Intel's CPUs and Xilinx's FPGAs).[115] All third parties which provided substantive responses, with the exception of one, have indicated that they do not expect the Proposed Transaction to increase the existing barriers to switching between different suppliers of CPUs and FPGAs.[116]

Multi-sourcing

75. Third party feedback also generally corroborates AMD's submissions that customers currently practise multi-sourcing[117] of both CPUs and FPGAs for various reasons including to encourage competition in quality and pricing amongst manufacturers[118] and to retain the ability to mix-and-match solutions to achieve optimal performance and efficiency levels for a given application[119]. (See paragraph 60 above)

Ability to negotiate prices

76. CCCS notes at the outset that the ability of the Parties' customers to negotiate prices is largely dependent on the commercial significance of the customer to the Parties (e.g. whether the customer is large or accounts for a significant portion of the revenue of the Parties) so as to be able to exert countervailing buyer pressure on the merged entity through the threat of switching (discussed above at paragraphs 73 to 74) or self-supply (discussed below at paragraph 77). In this

[115] All third parties indicated no difficulties, with the exception of one which stated that it is not in a position to comment. [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 15 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 35 to CCCS's 17 May 2021 RFI. [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021.

[116] All with the exception of [✂]. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 14 of CCCS's Invitation to Comment dated 17 May 2021. [✂]to Question 16 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 28 to CCCS's 17 May 2021 RFI.

[117] All third parties who responded indicated that they procure CPUs and FPGAs from multiple suppliers, with the exception of [✂]. [✂] to Question 15 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 15 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 13 of CCCS's Invitation to Comment dated 17 May 2021. [✂] response to Question 15 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 17 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 28 of CCCS's 17 May 2021 RFI.

[118] [✂] to Question 7 of CCCS's clarification questions dated 3 June 2021 to [✂] to CCCS's Invitation to Comment dated 17 May 2021.

[119] [✂] to Question 24 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 16 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 22(a) of CCCS's Invitation to Comment dated 17 May 2021.

regard, while some third party feedback corroborates AMD's submission that larger customers are able to exert influence on prices[120], some customers have expressed that they have no or limited bargaining power because their purchase volume is relatively low compared to other customers of the Parties[121]. Further, customers' ability to negotiate is also dependent on the overall market situation at any point in time (e.g. a worldwide shortage of wafers would limit the ability of customers to negotiate for better prices/terms of supply).

Ability to self-supply or sponsor entry

77. CCCS notes AMD's submission that self-supply is unlikely to be an economical choice for most smaller customers is generally corroborated by third party feedback.[122]

78. Given the above assessment, CCCS is of the view that there is no clear evidence to indicate that the customers of the Parties would be able to exercise significant buyer power. CCCS considers it is unnecessary to conclude whether customers of the Parties would be able to exercise significant buyer power, given its assessment that the merged entity is not likely to have the ability and incentive to bundle its products to enjoy significant portfolio power.

(d) Barriers to Entry and Expansion

79. Given the assessment above that the Proposed Transaction is unlikely to lead to SLC, CCCS is of the view that it is unnecessary to assess whether an entrant could replicate the merged entity's portfolio of products and sufficiently constrain the merged entity. However, for completeness, CCCS sets out its assessment on the barriers to entry and expansion below.

AMD's submissions

[120] [✂] to Question 23(c) of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 23(c) of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 23(c) of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 23 of CCCS's Invitation to Comment dated 17 May 2021.

[121] [✂] to Question 34(c) to CCCS's 17 May 2021 RFI. [✂] to Question 23(c) of CCCS's Invitation to Comment dated 17 May 2021.

[122] All third parties, with the exception of [✂], which were posed with that query responded that they are unable to self-supply CPUs and FPGA. [✂] to Question 26 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 26 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 26 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 26 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 37 to CCCS's 17 May 2021 RFI. [✂] to Question 26 of CCCS's Invitation to Comment dated 17 May 2021.

80. According to AMD, there are no significant factors that serve as barriers to entry for any of the products or services the Parties sell.[123] In particular, AMD has submitted that there is sufficient productive capacity within the semiconductor industry overall, and significant upfront investments in manufacturing facilities are generally not required to enter or expand into any of the Relevant Markets, even for new entrants.[124] This is due to the fact that semiconductor suppliers, including AMD[125] and Xilinx[126], commonly adopt a "fabless" model and outsource the production, assembly and testing of integrated circuits to independent third party suppliers (e.g. external foundries for wafer fabrication) which acts as a means to limit fixed investment costs.[127]

81. To the best of AMD's knowledge, these third party manufacturers do not suffer from capacity constraints.[128] AMD observed however that at the foundry level, production capacity is relatively fixed over the short term (one to two years), as capacity is planned several years in advance.[129] As a result of the investment and lead time required to increase wafer production capacity, short-term supply constraints can arise when demand unexpectedly increases beyond the available installed capacity.[130] However, third party wafer fabrication facilities, such as the Taiwan Semiconductor Manufacturing Company ("**TSMC**") and GlobalFoundries Inc., have indicated that they are investing in new production capacity to meet demand[131] as well as buildout leading edge process nodes capacity to address global chip shortage[132].

82. In this regard, AMD submitted that semiconductor companies such as Intel (also the largest competitor of the Parties in the Relevant Markets[133]) that both manufactures its own chips and outsources production to foundries would have far more control over prioritisation and production of its CPUs and FPGAs than

[123] Paragraph 28.1 of the Form M1.
[124] Paragraph 2.35 of AMD's 16 April 2021 Response to CCCS's 30 March 2021 Letter.
[125] Paragraph 1.2.1 of AMD's 16 April 2021 Response to CCCS's 30 March 2021 Letter. Please note that AMD primarily uses two foundries: GlobalFoundries Inc. and Taiwan Semiconductor Manufacturing Company, Limited.
[126] Paragraph 1.2.2 of AMD's 16 April 2021 Response to CCCS's 30 March 2021 Letter. Please note that Xilinx's FPGAs are manufactured by the following foundries: Taiwan Semiconductor Manufacturing Company, United Microelectronics Corporation and Samsung Electronics.
[127] Paragraphs 2.35 and 2.36 of AMD's 16 April 2021 Response to CCCS's 30 March 2021 Letter.
[128] Paragraph 2.36 of AMD's 16 April 2021 Response to CCCS's 30 March 2021 Letter.
[129] Paragraph 11.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[130] Paragraph 11.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[131] Paragraph 11.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[132] Paragraph 6.2 of Annex 2 of AMD's Response dated 28 July 2021 to CCCS's 2 July 2021 RFI.
[133] Paragraph 7.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

the Parties,[134] and do not face the same constraints of having to balance the demands of other companies as third party wafer fabrication facilities[135].

83. In relation to intellectual property rights, AMD has submitted that it is common in the semiconductor industry for companies to have numerous cross-licensing and technology exchange agreements with other companies under which they both transfer and receive technology and Intellectual Property Rights ("**IPRs**").[136] According to AMD, new entrants with sufficient capital and time would likely be able to obtain any cross-licensing or technology exchange agreement required to enter the relevant markets.[137]

84. The use of open standards, such as PCIe interconnect technology, also helps facilitate new entry by ensuring interoperability between the new entrant's device (e.g., FPGA) and other components in a computer system or server supplied by third parties.[138] AMD submitted that there are no other legal or regulatory barriers for new entrants to offer CPUs, FPGAs or any other products offered by the Parties.[139]

85. In terms of instances of market entry for CPUs, [✂].[140] AMD also notes that Nvidia has recently announced the NVIDIA Grace™ CPU, an ARM-based processor that is designed for data centres.[141] NVIDIA has stated it expects these CPUs to be available starting in 2023.[142]

86. There also exists a large number of technology companies of all sizes that could enter the markets for CPUs and FPGAs if they choose to devote resources, including engineering expertise, into this area.[143] For example, AMD notes that Apple created its own CPUs, the M1, for use in its own devices[144] and that Qualcomm recently acquired NUVIA which gives Qualcomm access to industry personnel who were involved in the creation of Apple's high-performance CPU cores.[145] [✂].[146]

[134] Paragraph 11.1 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[135] Paragraph 11.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[136] Paragraph 18.9 of Form M1.
[137] Paragraph 1.6 of AMD's Response dated 10 June 2021 to CCCS's 3 June 2021 RFI.
[138] Paragraph 18.10 of Form M1.
[139] Paragraph 18.11 of Form M1.
[140] Paragraph 2.37 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[141] Paragraph 12.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[142] Paragraph 12.2 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[143] Paragraph 2.38 of AMD's Response dated 16 April 2021 to CCCS's 30 March 2021 letter.
[144] Paragraph 12.5.4 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[145] Paragraph 12.5.5 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.
[146] Paragraph 12.5.5 of AMD's Response dated 26 May 2021 to CCCS's 7 May 2021 RFI.

CCCS's assessment

87. Feedback indicated that the barriers to entry for the supply of FPGAs to Singapore are high in view of the capital expenditure and the need to develop Intellectual Property ("**IP**") expertise, design and software development for the supply of FPGAs. [147] Similarly, for CPUs, feedback indicated that while entry into the relevant market for CPUs for data centres is possible due to the open licensing model of ARM's CPU architecture, it is difficult.[148] However, feedback indicates that the adoption of a fabless model may reduce the amount of fixed investment costs required for new entry and expansion by existing players.[149]

88. Notwithstanding the above, third party feedback indicates that there are potential new entrants in the Relevant Markets [150] some of whom may be currently developing their own ARM-based CPUs.[151]

89. CCCS notes that third party feedback generally corroborates AMD's submissions that new entry into the relevant market for the supply of CPUs and FPGAs to data centres is possible. CCCS further notes third party feedback that the need to ensure interoperability of a supplier's CPUs with FPGAs offered by other suppliers (and vice versa) is not a significant barrier to entry. Lastly, CCCS notes that the news reports corroborate AMD's submissions on [✂] NVIDIA's introduction of the Grace™ CPU. There does not seem to be any imminent entry into the market for FPGAs.

90. As regards expansion, CCCS notes that Intel, a key competitor of the Parties, has announced plans to invest US$20 billion to build two new factories to increase its production capacity.[152] CCCS further notes that the adoption of a fabless model may reduce the amount of fixed investment costs required for expansion of supply by existing suppliers, although the ability of existing suppliers to expand production of CPUs and FPGAs may still be limited by any supply constraints of

[147] [✂] to Question 21 of CCCS's Invitation to Comment dated 17 May 2021.
[148] [✂] to Questions 6 and 19 of CCCS's Invitation to Comment dated 17 May 2021.
[149] [✂] to Question 20 to CCCS's Invitation to Comment dated 17 May 2021.
[150] For CPUs, all respondents who provided substantive comments, with the exception of two respondents ([✂]), have indicated that entry is possible. For FPGAs, all respondents who provided substantive comments, with the exception of two respondents ([✂]) have indicated that entry is possible. Please see [✂]to Question 20 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Questions 13 and 18 to CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 18 of CCCS's 1 June 2021 Invitation to Comment. [✂] to Question 18 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 18 of CCCS's Invitation to Comment dated 17 May 2021. [✂] to Question 26 of CCCS's Invitation to Comment dated 17 May 2021.
[151] [✂] to Question 18 of CCCS's Invitation to Comment dated 17 May 2021.
[152] https://www.intel.com/content/www/us/en/newsroom/news/idm-manufacturing-innovation-product-leadership.html

wafers (a key input in the production of CPUs and FPGAs) by third party foundries.

91. CCCS considers it is unnecessary to definitively conclude whether the barriers of entry and expansion are likely to be high, given its assessment that the merged entity is not likely to have the ability and incentive to bundle its products to create such a portfolio of products that represents a strategic barrier to entry that would limit the ability of competitors to either enter or expand to compete with the merged entity.

92. Accordingly, CCCS maintains its assessment that the Proposed Transaction will not lead to a substantial lessening of competition resulting from the conglomerate effects arising from the merged entity supplying CPUs, discrete GPUs and FPGAs.

IX. EFFICIENCIES

AMD's submissions

93. AMD submitted that it expects to achieve approximately US$300 million (approximately S$396.63 million) of overall cost savings on an annualised basis within 18 months of closing the Proposed Transaction, primarily based on synergies in costs of goods sold, shared infrastructure and through streamlining common areas.[153]

94. Moreover, by combining the Parties' engineering teams and domain expertise (with a combined team of 13,000 talented engineers and over US$2.7 billion (approximately S$3.6 billion) of annual R&D investment), AMD hopes to accelerate technological development and create a company with the vision, talent and scale to compete in the future of high performance computing.[154]

CCCS's assessment

95. Given that the above competition assessment did not raise SLC concerns, CCCS is of the view that it is not necessary to make an assessment on the claimed efficiencies by AMD.

[153] Paragraph 42.1 of Form M1.
[154] Paragraph 42.2 of Form M1.

X. ANCILLARY RESTRICTIONS

96. AMD submitted that the Parties have not entered into any ancillary restrictions as part of the Proposed Transaction which may restrict competition[155] that would benefit from an exclusion from the application of the section 34 prohibition under the Act.[156]

XI. CONCLUSION

97. For the reasons above and based on the information available, CCCS assesses that the Proposed Transaction, if carried into effect, will not lead to an SLC and consequently, will not infringe the section 54 prohibition.

98. In accordance with section 57(7) of the Act, the decision will be valid for a period of one year from the date of CCCS's decision.

Sia Aik Kor
Chief Executive
for Competition and Consumer Commission of Singapore

[155] Paragraph 43.1 of Form M1.

[156] It is provided under paragraph 10 of the Third Schedule of the Competition Act (Cap. 50B) that the section 34 prohibition (prohibiting anticompetitive agreements and/or concerted practices) and the section 47 prohibition (prohibiting abuse of dominance) shall not apply to any agreement or conduct that is directly related and necessary to the implementation of a merger. Hence, CCCS requires merging parties to notify CCCS (via the Form M1) of any agreement/conduct that they would be entering into/carrying out as part of the anticipated merger/merger (i.e. termed "ancillary restrictions") that may potentially benefit from this exclusion.